IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Matthew J. Amatangelo, Jeannette N. Sutherland, Robert E. Mains		
Assignee:	Sun Microsystems, Inc.		
Title:	Static Timing Model for Combinatorial Gates Having Clock Signal Input		
Serial No.:	10/774,990	Filed:	February 9, 2004
Examiner:	Unknown	Group Art Unit:	2123
Docket No.:	P8900	Customer No.	33438

Austin, Texas
May 25, 2004

COMMISSIONER FOR PATENTS
PO Box 1450
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INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, Applicants wish to call the following documents to the attention of the Examiner.

A PTO form 1449 listing these documents is enclosed.

Citation of the above documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made, other than as described above; or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: COMMISSIONER FOR PATENTS, PO Box 1450, Alexandria, VA 22313-1450, on May 25, 2004.

Attorney for Applicant(s) — Date of Signature: 5/25/04

Respectfully submitted,

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Reg. No. 32,946

U.S. Department of Commerce, Patent and Trademark Office	Attorney Docket No.	Serial No.
	P8900	10/774,990
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant(s)	
(Use several sheets if necessary)	Matthew J. Amatangelo, et al.	
	Filing Date	Group
	February 9, 2004	2123

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AL						☐	☐
	AM						☐	☐
	AN						☐	☐

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AO	David Van Campenhout, Trevor Mudge, Karem A. Sakallah "Timing Verification of Sequential Domino Circuits," *Proc. TechCon 96*, September 1996
	AP	Pawan Kulshreshtha, Robert Palermo, Mohammad Mortazavi, Cyrus Bamji, Hakan Yalcin "Transistor-Level Timing Analysis Using Embedded Simulation" Cadence Design Systems, Inc. www.sigda.org/Archives/ ProceedingArchives/Iccad/Iccad2000/ papers/2000/iccad00/pdffiles/08a_3.pdf
	AR	Sumant Ramprasad, Ibrahim N. Hajj, Farid N. Najm "An Optimization Technique for Dual-Output Domino Logic," Proceedings 1999 International Symposium on Low Power Electronics and Design, p.258-260, August 16-17, 1999, San Diego, California
	AS	
	AT	

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.